REMARKS

I. Status of Application

Claims 14, 16 and 29-36 are all the claims pending in the application. Claims 14, 16 and 29-36 are rejected.

II. Objections to the Specification

The Examiner has objected to the specification alleging that the limitation "such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode" is not fully supported by a written description. Without conceding to the merits of the Examiner's objections, the specification has been amended, as set forth above. In view of the above amendments, Applicant respectfully requests that the Examiner withdraw these objections.

III. Claim Rejections Under 35 U.S.C. § 103

Claims 29, 16 and 34-36 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Prior Art as Admitted by Applicant (hereinafter "APA") in view of Osamu Nakamura (JP 2003-017502A) and Adler et al. (5,757,050). Claim 14 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura, in view of Adler, and further in view of Zhang al. (6,507,069). Claim 30 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura, in view of Adler, and further in view of Izawa et al. (5,053,849). Claims 31 and 32 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura, in view of Adler, and further in view of Numasawa et al. (6,048,795). Claim 33 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over APA, in view of Nakamura, in view of Adler, and further in view of Suzawa et al. (5,914,498). Applicant respectfully traverses all of these rejections.

Regarding independent claim 29, the Examiner acknowledges that APA fails to teach or suggest the claimed features of wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode. Nevertheless, the Examiner alleges that Nakamura remedies the deficient teachings of APA with respect to these features. Applicant respectfully disagrees with the Examiner's allegations as set forth in detail below.

First, the Examiner alleges that there is nothing in the inherent properties of an LDD, or any other impurity doping region contiguous with a region that is at least during the ON state electrically connecting the source and the drain, that precludes it from functioning as a channel region. Accordingly, the Examiner takes the position that any such region meets the requirements of the claimed "channel region."

Applicant respectfully disagrees with the Examiner's position in this regard. As an initial matter, the Examiner fails to provide any evidence in fact and/or reasoning to support his conclusory allegations that any such region meets the requirements of the claimed "channel region."[1].

Moreover, the Examiner is required to give the claims their broadest reasonable interpretation (*see* MPEP §2111.01). Applicant submits that one of ordinary skill in the art would not reasonably interpret the claimed channel region to include any impurity doping region

[1] "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (U.S. 2007).

contiguous with a region that is at least during the ON state, as alleged by the Examiner. Indeed, the Examiner seems to interpret the claimed "channel region" as being nothing more than an electron path and Applicant respectfully submits that such an interpretation is not reasonable as required by MPEP §2111.01. As such, the cited references fail to teach or suggest the claimed features for *at least* these reasons.

Second, the Examiner alleges that Drawing 4A and paragraphs 0058-0061 of Nakamura teach the features of a second active layer comprising a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity doping region disposed between said first and second channel regions such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode, as claimed. Along these lines, the Examiner alleges that the region marked P:5E19/cm^3 on the right side of Nakamura's Drawing 4A, or alternatively a sub-portion of the darkened region marked P:4E17/cm^3, are both positioned directly below the second gate electrode and, thus, correspond to the recited "first channel region." Further, the Examiner alleges that the region marked B:2E18/cm^3 of Nakamura's Drawing 4A corresponds to the claimed "second channel region."

Applicant respectfully disagrees with the Examiner's allegations. As shown in Drawing 4A of Nakamura, the semiconductor layer (polysilicon layer) consists of source and drain regions which are highly doped with n-type impurities (doped phosphorus (P) at a concentration of 5E19/cm^3 and these regions are referred to as "n^+ regions"). Nakamura's semiconductor layer also consists of LDD regions which are lightly doped with n-type impurities (doped phosphorus (P) at a concentration of 4E17/cm^3 and these regions are referred to as "n^- regions"). Moreover, Nakamura's semiconductor layer consists of a channel region which is slightly doped with p-

type impurities (doped boron (B) at a concentration of $2E16/cm^3$ and this region is referred to as a "p region" or an "i (intrinsic) region"). That is, Drawing 4A of Nakamura shows an "n-type field effect transistor (FET)."

As can be seen from the above description of Drawing 4A, Nakamura's channel region is completely different from the impurity doping regions in the dopant conductive type and the doping concentration. Therefore, no one skilled in the art would reasonably take the position that any of such impurity doping regions corresponds to a "channel region," as claimed. Furthermore, contrary to the reasoning applied by the grounds of rejection, one of ordinary skill in the art would have recognized that it is not necessary to use a transistor if it is always in an ON state. Accordingly, the cited references fail to teach or suggest the claimed features for *at least* these additional reasons.

Third, the Examiner alleges that the relative horizontal extent of LDD doping regions, such as the darkened region marked $P:4E17/cm^3$ in Nakamura, is an obvious matter of design choice. In particular, the Examiner alleges that Nakamura demonstrates that the feature of a non-overlapping portion of an LDD region is an obvious matter of design choice because both with and without this feature, the performance of the TFT substrate is qualified as useful (*see* Nakamura 0061). To further support his position, the Examiner relies on language from the recent KSR Int'l Co. v. Teleflex Inc. decision, alleging that claim 29 would have been obvious because one of ordinary skill has good reason to pursue the known options within his or her technical grasp, and if this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.

Again, Applicant respectfully disagrees. Contrary to the Examiner's allegations, Nakamura in no way demonstrates that the feature of a non-overlapping portion of an LDD

region is an obvious matter of design choice. In contrast, Nakamura clearly discloses that the electric field produced near the boundary of a channel formation field and an LDD field is eased. To obtain this effect, Nakamura teaches that the electrode 17 should be overlapped with gate electrode 13 as shown in all plan views, particularly Drawing 1A. That is, Nakamura teaches that the electrode 17 should be arranged over the boundary of the channel formation field and an LDD field. Indeed, Drawing 4A of Nakamura is nothing more than a schematic model. Therefore, Nakamura does not demonstrate that the feature of a non-overlapping portion of an LDD region is an obvious matter of design choice and cannot employ such a configuration.

In sharp contrast to Nakamura, according to an exemplary embodiment of the present invention shown in FIG. 11, the low voltage gate electrode 110 does not overlap LDD region 105f and the high voltage gate electrode 107 overlaps the LDD regions 105f and 105e. That is, the electric field is eased by a so-called LDD structure in the low voltage driving TFT including low voltage gate electrode 110 and a so-called GOLD structure in the high voltage driven TFT including high voltage gate electrode 107. As described with reference to an exemplary embodiment in paragraph 25 of the present specification, parasitic capacitance is more problematic in the low voltage driven TFT than in the high voltage driving TFT. Therefore, there can be formed a TFT substrate including a circuit which is constituted of plural kinds of TFTs with a high throughput and which can be driven at high speed with low power consumption. Furthermore, as described with reference to an exemplary embodiment in paragraph 35 of the present specification, a sub-gate structure in the high voltage driving TFT is excellent in output controllability at a low gate voltage, and therefore, is appropriate for a high withstand voltage TFT used for a level shift circuit. Applicant respectfully submits that such a sub-gate structure would not have been obvious from APA in view of Nakamura.

Therefore, claim 29 is patentable over the cited references for *at least* the above reasons. Moreover, the dependent claims 14, 16 and 30-36 are patentable *at least* by virtue of their dependency. Accordingly, Applicant respectfully requests that the Examiner withdraw these rejections.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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